IJREAT International Journal of Research in Engineering & Advanced Technology, Volume 1, Issue 4, Aug-Sept, 2013
ISSN: 2320 - 8791
www.ijreat.org

Low Power Negative Edge Triggered Flip-Flop Design

Sivasankar Kommala[1] , Gangavarapu Kiran kumar[2]

[1] **PG Student, M.Tech. (VLSI), Dept. of E.C.E., ASCET, JNTUA, Gudur, A.P, INDIA**

[2] **Associate Professor, Dept. of E.C.E., ASCET, JNTUA, Gudur, A.P, INDIA**

Abstract

In this paper a new technique is proposed based on the comparison between Conventional Transistorized Flip-flop and Data transition Look ahead D flip flop here we are checking the working of Low Power Pulse Trigger Flip-Flop with conditional pulse enhancement(PFF) and Implicit Pulsed Data Close to Output(IP-DCO) after that we are analyzing the characteristic comparison using power & area constraints after that we are proposing a flip-flop named as Low power Negative Edge Triggered Flip-Flop Design with reduced number of transistors which will reduce the overall power area as well as delay. The simulations are done using Microwind & DSCH analysis software tools and the result between all those types are listed below. Our proposed system simulations are done under 50nm technology and the results are tabulated below. In that our proposed system is showing better output than the other flip-flops compared here.

Keywords: *Flip-flop, Low Power, Pulse triggered, Edge triggered, DSCH, Microwind.*

1. Introduction

In electronics, a flip-flop or latch is a circuit that has two stable states and can be used to store state information. The circuit can be made to change state by signals applied to one or more control inputs and will have one or two outputs. It is the basic storage element in sequential logic. Flip-flops and latches are a fundamental building block of digital electronics systems used in computers, communications, and many other types of systems.

Flip-flops and latches are used as data storage elements. Such data storage can be used for storage of *state*, and

such a circuit is described as sequential logic. When used in a finite-state machine, the output and next state depend not only on its current input, but also on its current state (and hence, previous inputs). It can also Be used for

counting of pulses, and for synchronizing variably-timed input signals to some reference timing signal .Flip-flops can be either simple (transparent or opaque) or clocked (synchronous or edge-triggered); the simple ones are commonly called latches. The word *latch* is mainly used for storage elements, while clocked devices are described as *flip-flops*

.

D flip-flop

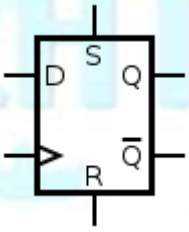


Figure 1: D flip-flop symbol

The D flip-flop is widely used. It is also known as a data or delay flip-flop.

The D flip-flop captures the value of the D-input at a definite portion of the clock cycle (such as the rising edge of the clock). That captured value becomes the Q output. At other times, the output Q does not change. The D flip-flop can be viewed as a memory cell, a zero-order hold, or a delay line.

Most D-type flip-flops in ICs have the capability to be forced to the set or reset state (which ignores the D and clock inputs), much like an SR flip-flop. Usually, the illegal S = R = 1 condition is resolved in D-type flip-flops. By setting S = R = 0, the flip-flop can be used as described above.

Types of D Flip-Flops

i. Classical Negative-edge-triggered D flip-flop
ii. Master–slave pulse-triggered D flip-flop
iii. Edge-triggered dynamic D storage element

2. Existing Systems

Some Flip-Flop designs, which are used as the reference designs in later performance comparisons, are first reviewed. A state-of-the-art P-FF design, named IP-DCO, is given in Figure 2.

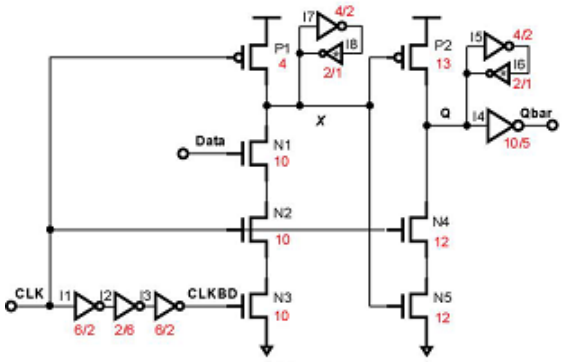
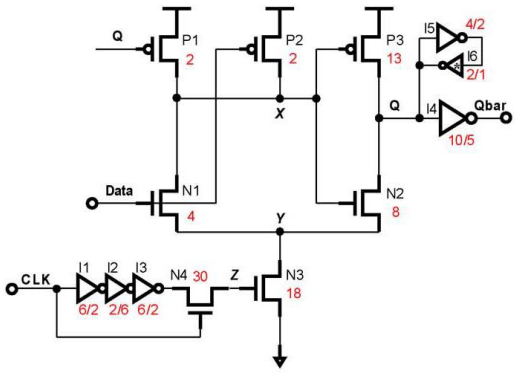


Figure 2:Circuit diagram of IP-DCO

It contains an AND logic-based pulse generator and a semi-dynamic structured latch design. Inverters I5 and I6 are used to latch data and inverters I7 and I8 are used to hold the internal node X. The pulse generator takes complementary and delay skewed clock signals to

Figure 3: Modified version of Hybrid Latch flip-Flop Circuit

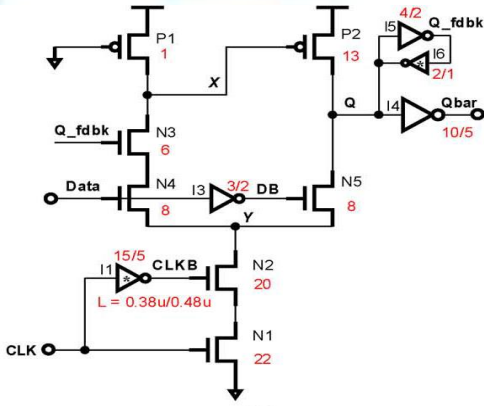


generate a transparent window equal in size to the delay by inverters I1-I3. Two practical problems exist in this design. First, during the rising edge, nMOS transistors N2 and N3 are turned on. If data remains high, node X will be discharged on every rising edge of the clock. This leads to a large switching power. The other problem is that node X controls two larger MOS transistors (P2 and N5). The large capacitive load to node X causes speed and power performance degradation.

Figure 3 shows an improved P-FF design, named Modified version of Hybrid Latch flip-Flop(MHLLF), by employing a static latch structure presented in Node X is no longer precharged periodically by the clock signal. A weak pull-up transistor P1 controlled by the FF output signal Q is used to maintain the node X level at high when Q is zero.

This design eliminates the unnecessary discharging problem at node X. However, it encounters a longer Data-to-Q (D-to-Q) delay during "0" to "1" transitions because node X is not pre-discharged. Larger transistors N3 and N4 are required to enhance the discharging capability. Another drawback of this design is that node X becomes floating when output Q and input Data both equal to "1". Extra DC power emerges if node X is drifted from an intact "1".

Figure 4 shows a refined low power P-FF design named 'Single Ended Conditional Capturing Energy Recovery (SCCER)' using a conditional discharged technique. In this design, the keeper logic (back-to-back inverters I7 and I8 in Fig. 2) is replaced by a weak pull up transistor P1 in conjunction with an inverter I2 to reduce the load capacitance of node X. The discharge path contains nMOS transistors N2 and N1 connected in series. In order to eliminate superfluous switching at node X, an extra nMOS transistor N3 is employed. Since N3 is controlled by Q-fdbk, no discharge occurs if input data remains high. The



worst case timing of this design occurs when input

Figure 4: SCCER Circuit

data is "1" and node is discharged through four transistors in series, i.e., N1 through N4, while combating with the pull up transistor P1. A powerful pull-down circuitry is thus needed to ensure node X can be properly discharged. This implies wider N1 and N2 transistors and a longer delay from the delay inverter I1 to widen the discharge pulse width

The design, as shown in Fig. 5 adopts two measures to overcome the problems associated with existing P-FF designs. The first one is reducing the number of nMOS

transistors stacked in the discharging path. The second one is supporting a mechanism to conditionally enhance the pull down strength when input data is "1." Refer to Fig. 5, the upper part latch design is similar to the one employed in SCCER design. As opposed to the transistor stacking design in Fig 2 and 4, transistor N2 is removed from the discharging path. Transistor N2, in conjunction with an additional transistor N3, forms a two-input pass transistor logic (PTL)-based AND gate to control the discharge of transistor N1. Since the two inputs to the AND logic are mostly complementary (except during the transition edges of the clock), the output node Z is kept at zero most of the time. When both input signals equal to "0" (during the falling edges of the clock), temporary floating at node Z is basically harmless.

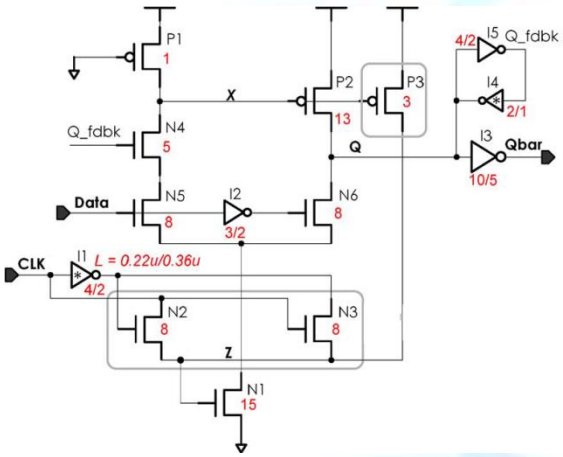


Figure 5: P-FF design with pulse control scheme

At the rising edges of the clock, both transistors N2 and N3 are turned on and collaborate to pass a weak logic high to node Z, which then turns on transistor N1 by a time span defined by the delay inverter I1. The switching power at node Z can be reduced due to a diminished voltage swing. Unlike the MHLLF design, where the discharge control signal is driven by a single transistor, parallel conduction of two nMOS transistors (N2 and N3) speeds up the operations of pulse generation. With this design measure, the number of stacked transistors along the discharging path is reduced and the sizes of transistors N1-N5 can be reduced also.

In this design, the longest discharging path is formed when input data is "1" while the Qbar output is "1." To enhance the discharging under this condition, transistor P3 is added. Transistor P3 is normally turned off because node X is pulled high most of the time. It steps in when node X is discharged to V_{TP} below the V_{DD}. This provides additional boost to node . The generated pulse is taller, which enhances the pull-down strength of transistor N1. After the rising edge of the clock, the delay inverter I1 drives node Z back to zero through transistor N3 to shut down the discharging path.

The voltage level of Node X rises and turns off transistor P3 eventually. With the intervention of P3, the width of the generated discharging pulse is stretched out. This means to create a pulse with sufficient width for correct data capturing, a bulky delay inverter design, which constitutes most of the power consumption in pulse generation logic, is no longer needed. It should be noted that this conditional pulse enhancement technique takes effects only when the FF output Q is subject to a data change from 0 to 1. The above existing FF designs contain more transistors and large number of clocked transistors. It consumes more power and area.

3. Proposed design

Reducing the Power and Area Proposing a less number of transistors design, Edge-triggered flip-flops are becoming a popular technique for low-power designs since they effectively enable a halving of the clock frequency. A dual pulse clock generator is needed to generate pulses at both rising and falling edges of a low-swing clock. This Particular clock pulse is used to switch the ground of the flip-flop circuit. This ground will be utilized by the NMOS and PMOS connected directly to the D input of the circuit. The Proposed system is shown in the figure below.

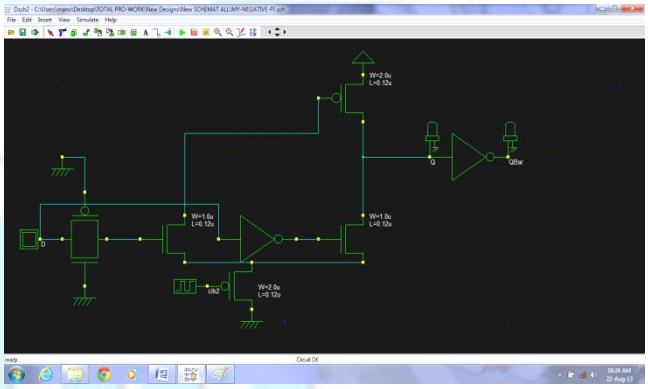


Figure 6: Proposed low power Flip Flop design

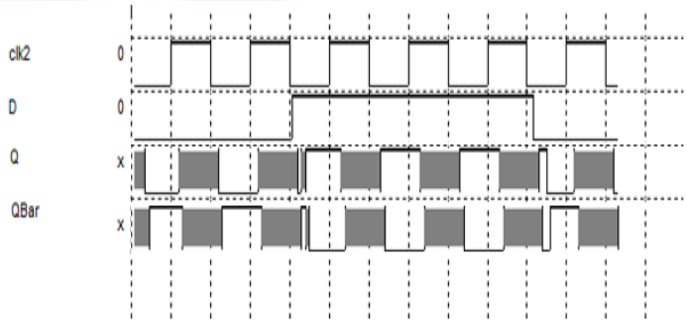


Figure7: Proposed Design Simulation Waveform Results

By using the Transistor switching logic only we are designing this circuit so it will be consuming only less power when compared to all other circuits. As well as we are having only 8 Transistors including the not gates also. So we will be having much reduced power and area when compared to the other two designs. At the same time due to the reduced no of transistor count we can reduce the delay oriented things also. Thus we are reducing the overall switching delay and power, area consumption.

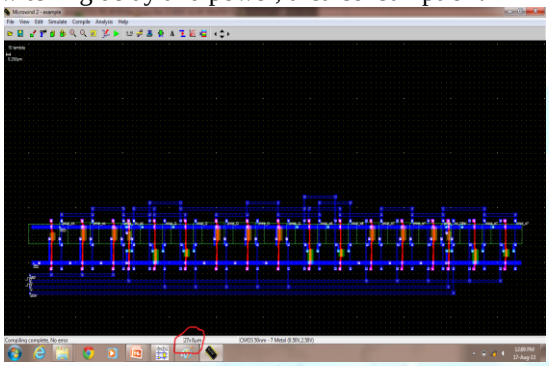


Figure 8: Layout of the Design(Area)

The graph in figure 7 represents the input & output characteristics of our proposed system from that we can clearly understand how it works as negative edge triggered flip-flop. There is some nano seconds delay is there even though it's a negligible amount only. Those delays can be further reduced by reducing the sizes of the transistor we are using in this circuit. Or by reducing the nano meter design of the proposed new flip-flop is shown in the figure 8 the area of that is mentioned at the downside of the layout. The Power consumption characteristics also mentioned below in figure 9.

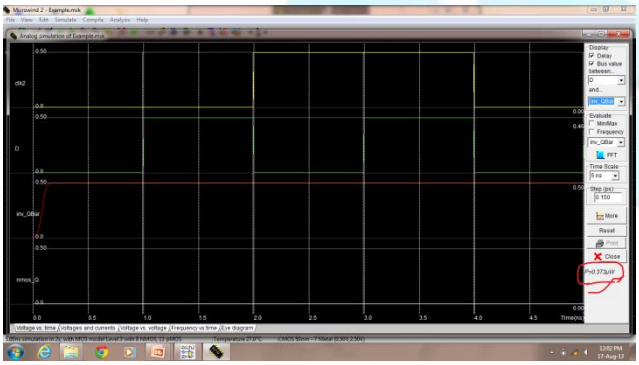


Figure 9: Power characteristic of the proposed design

Comparison of Flip-Flop Design Results (50Nm)

Flip - FlopType	*Power Consumption(µw)*	*Area Consumption(µm-^{2})*
IP-DCO	*0.867*	*185*
TGFF	*0.721*	*260*
PFF with pulse control scheme	*0.958*	*185*
Proposed Flip-Flop design	*0.373*	*162*

4. Conclusion

In this Paper, the various Flip-Flop designs like TGFF, Ip-DCO, PFF and proposed flip- flop design are discussed. The flip-flops were been designed in DSCH and Microwind tool in 50nm compared. The Proposed system shows 60%-70% Power improvement than the Existing Pulse trigger flip-flop with pulse control scheme and IP-DCO and it shows an improvement of 25%-35% in area constraints. Thus our proposed system is having very less power and area constraints which will lead to improvement in the case implementation in future mobile devices. This can be much suitable for application of battery oriented operation for less power and area. In future we can add some other leakage reduction techniques and the power can be further reduced.

References

[1] F. Klass, C. Amir, A. Das, K. Aingaran, C. Truong, R.Wang, A. Mehta,R. Heald, and G.Yee, "A new family of semi-dynamic and dynamic flip-flops with embedded logic for high-performance processors," *IEEE J.Solid-State Circuits*, vol. 34, no. 5, pp. 712–716, May 1999.

[2] S. D. Naffziger, G. Colon-Bonet, T. Fischer, R. Riedlinger, T. J.Sullivan, and T. Grutkowski, "The implementation of the Itanium 2microprocessor," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp.1448–1460, Nov. 2002.

[3] J. Tschanz, S. Narendra, Z. Chen, S. Borkar, M. Sachdev, and V. De,"Comparative delay and energy of single edge-triggered and dual edge triggered pulsed flip-flops for high-performance microprocessors," in *Proc. ISPLED*, 2001, pp. 207–212.

[4] B. Kong, S. Kim, and Y. Jun, "Conditional-capture flip-flop for statistical power reduction," *IEEE J. Solid-State Circuits*, vol. 36, no. 8, pp.1263–1271, Aug. 2001.
[5] N.Nedovic, M. Aleksic, and V. G. Oklobdzija, "Conditional precharge techniques for power-efficient dual-edge clocking," in *Proc. Int. Symp.Low-Power Electron. Design*,Monterey, CA, Aug. 12–14, 2002, pp.56–59.
[6] P. Zhao, T. Darwish, and M. Bayoumi, "High-performance and low power conditional discharge flip-flop," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 12, no. 5, pp. 477–484, May 2004.
[7] H. Mahmoodi, V. Tirumalashetty, M. Cooke, and K. Roy, "Ultra low power clocking scheme using energy recovery and clock gating," *IEEETrans. Very Large Scale Integr. (VLSI) Syst.*, vol. 17, pp. 33–44, Jan.2009.
[8] P. Zhao, J. McNeely, W. Kaung, N. Wang, and Z. Wang, "Design of sequential elements for low power clocking system," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, to be published.
[9] Y.-H. Shu, S.Tenqchen, M.-C. Sun,and W.-S. Feng, "XNOR-based double-edge-triggered flip-flop for two-phase pipelines," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 53, no. 2, pp. 138–142, Feb. 2006.
[10] V. G. Oklobdzija, "Clocking and clocked storage elements in a multigiga-hertz environment," *IBM J. Res. Devel.*, vol. 47, pp. 567–584, Sep.2003.

ABOUT AUTHORS

SIVASANKAR KOMMALA is M. Tech Post-Graduate of VLSI from Audisankara College of Engineering and Technology (ASCET), Gudur, Department of ECE, JNTUA. He obtained his B.Tech from Narayana of Engineering College (NECG), Gudur, AP. His interesting fields are Core VLSI, Low power Chip Design, Analog & Digital VLSI and Testability Issues.

GANGAVARAPU KIRAN KUMAR is working as Assoc. Professor in ECE Dept. Audisankara College of Engineering and Technology (ASCET), Gudur. He has been guiding U.G. &P.G. projects since six years in this institution. He also presented papers in seven international journals and six international conferences. His interesting Fields are Core VLSI, Analog & Digital VLSI, Embedded Systems and Testability Issues.